ABSTRACT

0026 A method for forming triple polysilicon split gate electrodes in a EEPROM flash memory array providing a first gate structure; blanket depositing a first polysilicon layer over the first gate structure; etching back the first polysilicon layer according to a first dry etching process; blanket depositing a second dielectric insulating layer over the first polysilicon layer; blanket depositing a second polysilicon layer over the second dielectric insulating layer; and, lithographically patterning and dry etching according to a respective third and fourth dry etching process through a thickness portion of the respective second and first polysilicon layers to respectively form third and second polysilicon gate electrodes.